



LISTING OF CLAIMS

1. (Previously presented) A circuit card comprising:

a circuit element supported by the circuit card, the circuit element having a plurality of inputs and outputs;

a plurality of signal lines supported by the circuit card, each signal line being electrically connected respectively to one of said plurality of inputs or one of said plurality of outputs; and

a plurality of shields supported by the circuit card;

wherein said signal lines are grouped in a plurality of adjacent corresponding pairs, a shield being located respectively on each side of each of said plurality of corresponding pairs of said signal lines.
2. (Previously presented) The circuit card according to claim 1, wherein each said shield is a ground shield.
3. (Previously presented) The circuit card according to claim 1, wherein said circuit element further comprises:

a driver to drive signals between said inputs and said outputs of said circuit element.
4. (Previously presented) The circuit card according to claim 1, wherein said signal lines are arranged and configured such that signals in each of said corresponding pairs of signal lines are differential signals.
5. (Previously presented) The circuit card according to claim 1, wherein said circuit element is a memory device.

6. (Previously presented) A circuit card comprising:

a plurality of signal lines supported by the circuit card, each signal line being arranged and configured to be electrically connected at a first end respectively to one of a plurality of connectors of a connector device mounted on a printed circuit board;

a circuit element mounted to the circuit card and having a plurality of inputs and outputs, said signal lines being electrically connected at a second end respectively to one of said plurality of inputs or outputs; and

a plurality of shields supported by said circuit card, the shields being arranged and configured on said circuit card to be electrically connected at a first end to respective connectors of said connector device mounted on said printed circuit board, each shield being electrically connected at a second end to a respective one of said plurality of circuit element inputs or outputs;

said signal lines being grouped in a plurality of adjacent corresponding pairs, respective ones of said shields being located on each side of each of said plurality of corresponding pairs of said signal lines.

7. (Previously presented) The circuit card according to claim 6, wherein said shields are ground shields.

8. (Previously presented) A circuit card comprising:

a plurality of signal lines on the circuit card and having a length arranged and configured to connect between a connector device and a circuit element, supported by the circuit card, to conduct signals therebetween, said plurality of signal lines being grouped in adjacent corresponding pairs; and

a shield on the circuit card extending adjacent and the length of each respective signal line pair;

wherein said signal lines are part of a bus system.

9. (Previously presented) The circuit card according to claim 8, wherein said shields are ground shields.

10. (Previously presented) The circuit card according to claim 8, wherein said circuit element has inputs and outputs for differential signals and said signal lines are arranged and configured such that signals transmitted in each of said corresponding pairs are differential signals.

11. (Previously presented) A memory expansion card comprising:
a memory device supported by the expansion card and having a plurality of inputs and outputs;

a plurality of signal lines supported by the expansion card, each of said plurality of inputs and outputs of said memory device being coupled to a respective one of said signal lines, said signal lines being grouped in a plurality of adjacent corresponding pairs; and

a plurality of shields on the expansion card and electrically connected to said memory device, a shield being located respectively between each pair of said plurality of corresponding pairs of said signal lines;

wherein said plurality of signal lines is part of a bus system.

12. (Previously presented) The memory expansion card according to claim 11, wherein each said shield is a ground shield.

13. (Previously presented) The memory expansion card according to claim 11, wherein signals to be transmitted in each of said corresponding pairs of adjacent signal lines are differential signals.

14. (Previously presented) The memory expansion card according to claim 11, wherein said expansion card is adapted for connection to a motherboard.

15. (Previously presented) A memory expansion card comprising:

a memory device supported by said expansion card and having a plurality of inputs and outputs;

a plurality of signal lines supported by said expansion card, each signal line connected respectively to one of said inputs or outputs, said plurality of signal lines being grouped respectively in adjacent corresponding pairs; and

a plurality of shields supported by said expansion card and electrically connected to said memory device, respective ones of said plurality of shields being located to extend along and between each of said plurality of corresponding pairs of said signal lines;

wherein said plurality of signal lines is part of a bus system.

16. (Previously presented) The memory expansion card according to claim 15, wherein each said shield is a ground shield.

17. (Previously presented) The memory expansion card according to claim 15, wherein said signal lines are arranged and configured such that signals transmitted in each of said corresponding pairs are differential signals.

18. (Previously presented) A memory expansion card assembly comprising:

a connector device mounted on a motherboard and having a plurality of connectors, said plurality of connectors having a first portion for conducting signals and a second portion for providing a shield, said connectors in said first portion being grouped in a plurality of corresponding pairs, a respective one of said connectors in said second portion being located between each of said plurality of corresponding pairs of said first portion of said plurality of connectors;

a plurality of signal lines on said expansion card being connected respectively to each of said first portion of connectors; and

a plurality of shields on said expansion card being connected respectively to each of said connectors in said second portion and extending respectively along adjacent signal lines connected to said first portion of connectors,

wherein said first portion of connectors is part of a bus system.

19. (Previously presented) A processing system comprising:

a processing unit;

a connector device having a plurality of pins and electrically connected to said processing unit and

a circuit card coupled to said processing unit through said connector device, said circuit card comprising:

a circuit element supported by the circuit card and having a plurality of inputs and outputs;

a plurality of signal lines supported by the circuit card, each of said plurality of signal lines being coupled respectively between one of said plurality of

inputs and one of said plurality of pins, or one of said plurality of outputs and one of said plurality of pins; and

a plurality of shields supported by the circuit card, each shield being connected respectively to said circuit element, said signal lines being grouped in a plurality of adjacent corresponding pairs, a shield being located between respective corresponding pairs of said signal lines;

wherein said processing system comprises a bus system for passing signals through said processing system and said signal lines are coupled to said bus system.

20. (Previously presented) The processing system according to claim 19, wherein each said shield is a ground shield.

Claim 21. (Canceled)

22. (Previously presented) The processing system according to claim 19, wherein said circuit element further comprises:

a driver to drive signals between said inputs and said outputs of said circuit element.

23. (Previously presented) The processing system according to claim 19, wherein said circuit element has inputs and outputs for differential signals and said signal lines are arranged and configured such that signals transmitted in each of said corresponding pairs are differential signals.

24. (Previously presented) The processing system according to claim 19, wherein said circuit element is a memory device.

25. (Previously presented) The processing system according to claim 19, wherein said processing unit and said circuit element are on a same chip.

26. (Previously presented) A processing system comprising:

a processing unit; and

a memory expansion card coupled to said processing unit, said memory expansion card comprising:

a memory device supported on said memory expansion card and having a plurality of inputs and outputs;

a connector device having a plurality of connectors for electrically coupling said memory expansion card to said processing unit; and

a plurality of signal lines and a plurality of shields supported by said memory expansion card, each of a first portion of said plurality of inputs and outputs of said memory device being coupled to a respective signal line to receive signals from or send signals to respective ones of said connectors of said connector device, said signal lines being grouped in a plurality of corresponding pairs, a shield being located on each respective side of each of said plurality of corresponding pairs of said signal lines;

wherein said processing system comprises a bus system for passing signals through said processing system and wherein said first portion of said plurality of inputs and outputs is coupled to said bus system.

27. (Previously presented) The processing system according to claim 26, wherein said shields are ground shields.

28. (Previously presented) The processing system according to claim 26, wherein said signal lines are arranged such that signals in each of said corresponding pairs are differential signals.

29. (Previously presented) The processing system according to claim 26, further comprising:

a motherboard equipped with a connector adapted for connection of said memory expansion card to said motherboard, the connector comprising connecting pins corresponding respectively to said signal lines and said shields.

30. (Previously presented) A processing system comprising:

a processing unit; and

a memory expansion card coupled to said processing unit, said memory expansion card comprising:

a memory device having a plurality of inputs and a plurality of outputs;

a plurality of signal lines supported by said expansion card and connected respectively to said plurality of inputs and outputs, said plurality of signal lines being grouped in a plurality of adjacent corresponding pairs; and

a plurality of shields supported by said expansion card and electrically connected to said memory device, a respective one of said plurality of shields being located to extend along each of said plurality of corresponding pairs of said plurality of signal lines;

wherein said plurality of signal lines is part of a bus system of said processing system.

31. (Previously presented) The processing system according to claim 30, wherein said shields are ground shields.

32. (Previously presented) The processing system according to claim 30, wherein said signal lines are arranged such that signals in each of said corresponding pairs are differential signals.

33. (Previously presented) A method for constructing on a circuit card a bus system device comprising the steps of:

providing a circuit element on said circuit card, said circuit element having a first plurality of connectors for conducting bus signals;

grouping said first plurality of connectors into a plurality of corresponding pairs; and

providing a second plurality of connectors on said circuit element, said second plurality of connectors being connected to a respective shield supported on said circuit card and extending along each side of respective pairs of signal lines supported on said circuit card and connected to each of said corresponding pairs of said first plurality of connectors.

Claim 34. (Canceled)

35. (Previously presented) The method according to claim 33, further comprising adapting said first plurality of connectors in each corresponding pair to conduct differential signals.